New Architecture for EIA-709.1 Protocol Implementation

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***Abstract* — This paper proposes a new architecture for EIA-709.1 protocol implementation. The protocol is conventionally implemented with the proprietary processor and language, Neuron chip and Neuron C, respectively, where the Neuron chip consists of 3 processors inside. The proposed architecture uses only one general purpose processor and general ANSI C to implement the layers of EIA-709.1 except the physical layer. The data link, network, and other layers are implemented onto one RISC processor, ARM. Specifically, the data link layer of the EIA-709.1 based on predictive p-persistent CSMA/CA is implemented. The interface between the transceiver based on power line communication and the data link layer based on the ARM is described. As a conclusion, this research shows the improvement of performance and the compatibility with the existing Neuron chip.**

Keywords-componen t; Architecture, EIA-709.1, Neuron chip, Neuron C, Power Line Communication

I. INTRODUCTION

LonWorks is a networking platform which is specifically designed for open and distributed control applications by Echlon Corporation. The platform consists of LonTalk communication protocol and firmware of Neuron chip, networking media such as twisted pair, power lines, fiber optics, and RF, and LonWorks Network Services. It is used for the automation of various functions in industrial control, home automation, transportation and building systems such as lighting and HVAC,.

The LonTalk[1] communication protocol which is part of the LonWorks was designed specifically for open and interoperable control system networks and provides for peer-to-peer communications between devices manufactured by different suppliers. Devices incorporating the LonTalk technology provide the interconnectable components required for an interoperable system. The LonTalk protocol is based on an enhanced CSMA network access algorithm which provides for a collision avoidance scheme.

Even though LonTalk technology based on Field Bus in control system has been widely used in the area of industrial automation for several years[2], it has some serious problems for implementing large size algorithm and high performance applications because of the limitations of the Neuron chip[1][3]. Even though the LonTalk is open-standard protocol of ANSI Standard ANSI/EIA 709.1, the flexibility of the LonTalk system is diminished from the use of both the specific Neuron chip and the specific software (Neuron C).

Currently, all the OSI seven layers of EIA 709.1 protocol are implemented on one Neuron chip which consists of three processors. The Neuron chip contains three 8-bit central processing units (CPUs) for MAC layer, network layer and application layer of EIA 709.1 protocol as seen in Fig. 1. Each of the three CPUs has its own register set, but all three CPUs share memory and address ALUs through pipelines. Access to BUS is mediated with semaphores to resolve contention when updating shared data.

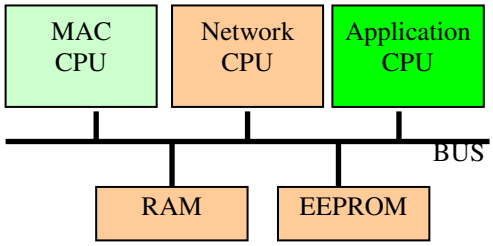

Figure 1. Block diagram of the Neuron chip

The Media Access Control (MAC) CPU handles layers one and two of the seven-layer EIA 709.1 protocol stack and includes driving the communication sub-system hardwares as well as executing the media access algorithm.

The Network CPU implements layers, layer three to six of the EIA 709.1 protocol stack. It handles network variable processing, addressing, transaction processing, authentication, background diagnostics, software timers and network management. An application CPU runs code written by the user, together with the operating system services called by applications code written by Neuron C.

There were some works to compensate and overcome the limitation of the Neuron chip. Basically, researchers wanted to take the advantages of the open protocol. Adept System Inc [4] has developed the protocol based on Motorola MC68360. Loytec [5] has developed based on ARM 7. Kim [6] has the developed the protocol based on embedded Linux platform that

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MAC layer and physical layer are implemented on external device and rests of upper layers are implemented on Linux. Choi [7] has developed the protocol based on FPGA using VHDL.

II. THE PROPOSED ARCHITECTURE FOR EIA 709.1

This paper proposes to use just both one general high performance processor and general ANSI C. The proposed architecture for EIA 709.1 protocol layers is illustrated in Fig. 2. The processor contains all the protocol stacks up to the layer seven above a transceiver. And EIA 709.1 protocol is implemented with ANSI C instead of Neuron C. This architecture can improve the flexibility of the Lontalk node with EIA 709.1 protocol and also can enhance the processing capability from the 32bit processor rather than using 8-bit microprocessor.

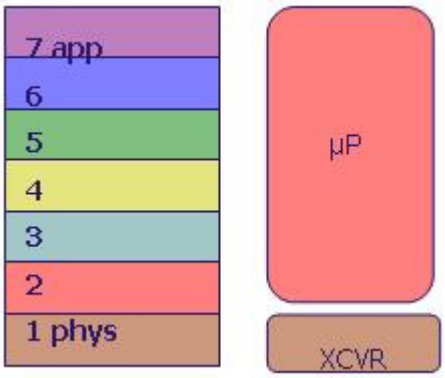

Figure 2. The prosed architecture for EIA-709.1

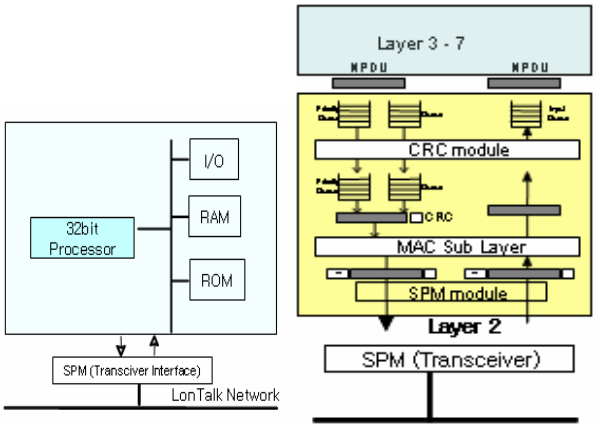

Figure 3. The Proposed architecture hardware/software

Fig. 3 shows the hardware and software configuration for the proposed system. The hardware system consists of one 32-bit ARM processor, RAM, and ROM, etc. The software system for the protocol consists of OSI 7 layers from physical to application layer. Especially, the data link layer consists of MAC sub layer, CRC module, send/receive buffer, and SPM interface module, etc. The every node of EIA-709.1 is physically connected to a channel with a transceiver that supports the physical layer. EIA 709.1 protocol is media independent; multiple physical layer protocols are supported depending on the communication media (twisted-pairs, coaxial cables, optical fibers, power lines, etc.). In this proposed architecture, the various communication media can be interfaced through SPM by selecting an appropriate media transceiver in EIA 709.1 approved-channel.

III. IMPLEMENTATION OF THE PROPOSED ARCHITECTURE

For the implementation of the proposed architecture, approved-transceiver, PLT-22 [8], which is Echelon's transceiver for power line communication is used as both the physical layer and the medium. An implemented example of the proposed system is illustrated in Fig. 4. The developed board also includes a 32bit processor, S3C2410 [9] of Samsung with built-in ARM 9 core and SPM module. The data link layer and the other upper layers of the EIA 709.1 protocol can be ported in ROM on the board.

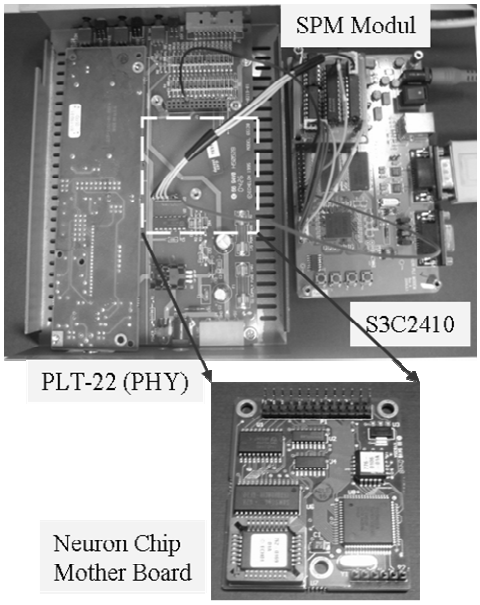

Figure 4. Developed S3C2410 board and Neuron board

A. *Implementation of SPM Iinterface*

For the power lines, the SPM [10] is used as the interface between power line transceiver, PLT-22, and the ARM processor. The standard SPM (Special Purpose Mode) communication is required as the interface between the data link layer and the PLT-22 transceiver for EIA-709.1

The SPM interface requires 4 I/O ports such as frame clock, bit clock, Rx, and Tx. However, S3C2410 does support SPI interface instead of SPM. SPI has the following 4 I/O signal lines: SPICLK, SPIMOSI, SPIMISO, and nSS. Because of the different signal configurations between SPI and SPM, a digital conversion logic circuit between them is designed and developed as illustrated in Fig.5.

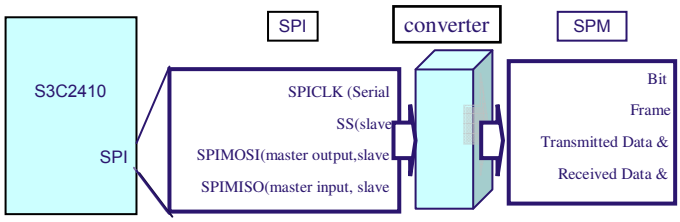

Figure 5. Converter between SPI and SPM

B. Implementation of Data Link Layers

As shown in Fig. 3, there are two output queues in the data link layer for priority algorithm, such as output and output-priority queues. The CRC for outgoing packets is computed in the layer 2. But, for incoming packets, the CRC computation is done by the MAC layer as bytes are received one by one in the special purpose mode. The reason is due to the fact that MAC sub layer needs to know whether the packet received has valid CRC or not and the backlog value in the packet to implement the channel access algorithm correctly. The polynomial $X^{16} + X^{12} + X^5 + 1$ (the CCITT CRC-16 standard) is used for error checking. MAC sub layer uses the predictive p-persistent CSMA algorithm and SPM interface for data handshaking.

The layer 2 including MAC layer has been implemented by using ANSI C. ADS1.2 of Metrowerks ltd. is used to compile the program source. As a result, the total compiled program size is about 28 KB. But it is not an optimized code size.

IV. TEST AND RESULTS

The test for SPM is first verified. Fig. 6 shows the comparison of SPM signals for Neuron and the proposed node. MAC in Neuron chip is independently operated and controlled from one of 3 8-bit processors. So, data transmission is made without any interruption between clock signals for Neuron node. However, MAC and other operations in the proposed architecture are supported only with an interrupt service routine (ISR) between services based on one 32-bit processor. Because of high speed processor usage, overall performance and speed is much better than Neuron even though the ISR service may cause delay. In an initialization process, Neuron and S3C2410 take time of 1.012ms and 224.9 μ s, respectively.

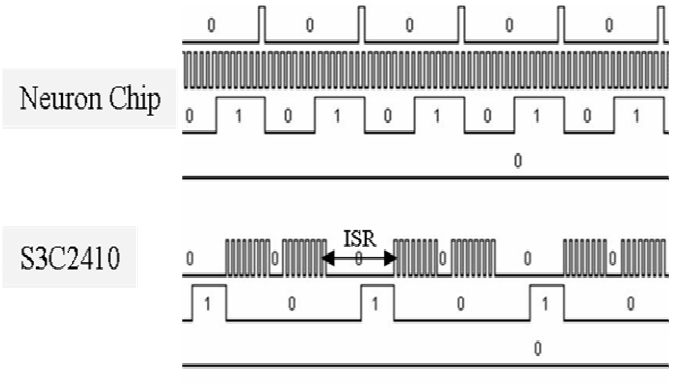

Figure 6. SPM Signal comparison

For the interoperability and performance of the implemented system, concept of the test is made as shown in Fig. 7. The proposed and Neuron node are connected through power lines in order to test. Protocol layers for EIA-709.1 are implemented onto the each node.

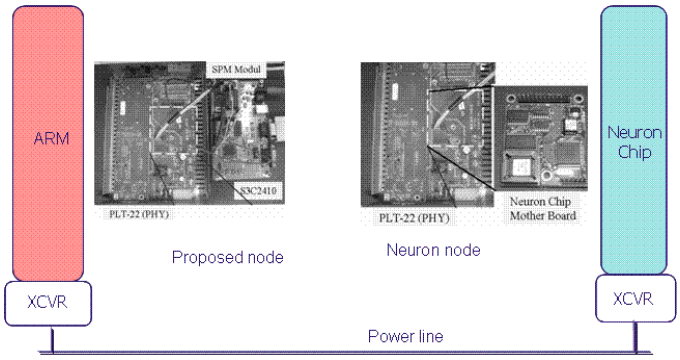

Figure 7. Experiment concept for interoperability

Fig.8 shows an actual experiment setup used for the interoperability. For layer 2 function tests, we have sent NPDU packets from ARM processor to the transceiver for the initialization of the transceiver. Then, another board receives the packet. While transferring the packet, the link layer frame is analyzed using EIA 709.1 protocol analyzer software. We have succeeded to check the information of layer 2 protocol including priority, backlog, alt path, L2Hdr and CRC status. Also, we have successfully received the corresponding ACK-bits from the transceiver, which tells that both the implemented system and the existing Neuron system can communicate each other.

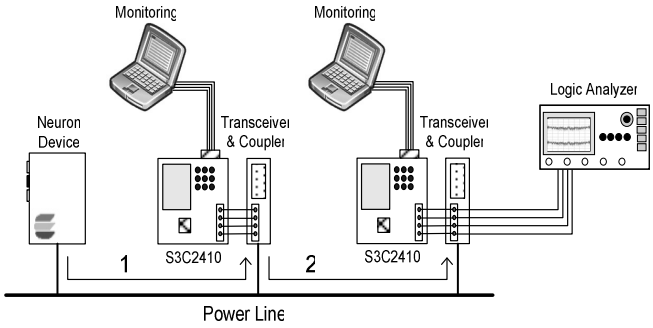

Figure 8. Test setup for EIA 709.1 protocol

A service test pin on the Neuron device is used for another test, where information such as Neuron ID and program ID of EIA 709.1 devices can be sent with the help of the service pin push. After receiving the packet through the implemented system, the analysis of the packet has been proved to be compatible with the existing EIA 709.1' devices in the MAC layer.

Reversely, packets transmitted from the implemented system have been rightly recognized from the existing Neuron device, which is analyzed with the help of the EIA 709.1 protocol analyzer of Echelon. From the analysis, we have

confirmed that the developed protocol has been interoperable with EIA 709.1.

V. CONCLUSIONS

In this paper, problems of the EIA-709.1 protocol implementation with the proprietary Neuron chip and Neuron C are discussed. The new architecture for EIA 709.1 implementation is proposed to improve performance from the 32bit processor rather than using 8-bit microprocessor, and proposed to enhance extensibility by using a general purpose processor and general programming language.

For the implementation of the layers of the protocol, the data, network, and other layers are implemented onto the 32bit S3C2410, ARM 9 and ANSI C. For the physical layer, the transceiver based on power line communication is used. The converter logic is developed for the interface, because of discrepancy between SPI provided by ARM processor and SPM supported by EIA-709.1.

After the implementation of the proposed architecture, the interoperability of the proposed system with existing EIA 709.1 network devices is confirmed from the test through power line. The results show that the communication performance between data link layer and physical layer is improved. Consistent network performance is accomplished without degradation due to heavy network traffic.

As a conclusion, the proposed architecture can improve flexibility and decrease costs of the development for the EIA-709.1 system. Also, the proposed system will be suitable for the system requiring high performance processing, and make the best use of open-standard protocol.

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